**September 23rd Senior Project Meeting**

**Armstrong Hall 137: 3:30-4:00 P.M.**

**Members in Attendance:** Dr. Orlando Hernandez, Zachary Nelson, Julie Swift, Dhruvit Naik and Kevin Cao

**Last Week’s Work:**

* Zach
  + Cleaned up RTS/RTR and XFC Protocols
  + Updated CORE 9 Files
  + Updated Schedule on Microsoft Project
    - Everyone agreed on due dates
    - Created a calendar on Google
  + Continued working on i2si\_bist\_gen.v
* Kevin
  + Continued working on i2si\_deserializer.v
  + Looked into setting up the project website
* Dhruvit
  + Continued working on filter\_convolution.v
* Julie
  + Continued working on register block document and register.v
* Whitley
  + Continued working on i2c\_slave\_deserializer.v

**Next Week’s Due Dates:**

* Friday, September 25th
  + Install Linux on Machine in Room 144B (Dhruvit and Julie)
* Monday, September 28th
  + Finish Design and Testing: filter\_convolution.v (Dhruvit)
  + Install EDA Tool on Machine in Room 144b (Dhruvit)
* Wednesday, September 30th
  + Finish Design and Testing: i2c\_salve\_deserializer.v (Whitley)
  + Finish Design and Testing: i2si\_bist\_gen.v (Zach)
  + Finish Design and Testing: i2si\_deserializer (Kevin)

**Meeting Notes:**

* We should have a testing specification when we perform testing
  + Multiple smaller unit tests are better than a couple of large comprehensive tests for our blocks
* Dr. Hernandez offered to present his presentation slides on Verilog to the group
  + All of the Verilog modules will have 3 always statements
  + The group will look over the slides and let Dr. Hernandez know if this will be beneficial
  + These slides would take approximately 6 hours in total to go through